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October 23, 2003

MS APPEAL BRIEF-PATENTS
COMMISSIONER FOR PATENTS
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Attn: Board of Patent Appeals and Interferences

Re: Patent Application of Mika SHIIKI et al.
Serial No. 09/916,527
Filed: July 27, 2001
Group Art Unit - 2822
Examiner: Kiesha L. Rose
Docket No. S004-4335

S I R:

Appellants submit herewith, in triplicate, their brief on appeal in connection with the captioned application. A check in the amount $330.00 is enclosed herewith to cover the required appeal fee. Should the check prove insufficient for any reason, authorization is hereby given to charge any deficiency to Deposit Account No. 01-0268.

Respectfully submitted,

ADAMS & WILKS
Attorneys for Appellants

By: _____
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BLA:db
Enclosures

MAILING CERTIFICATE

I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: MS APPEAL BRIEF-PATENTS, COMMISSIONER FOR PATENTS, P.O. Box 1450, Alexandria, VA 22313-1450, on the date indicated below.

Debra Buonincontri
Name

Debra Buonincontri
Signature

October 23, 2003
Date

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

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Application of	:	
Mika SHIIKI et al.	:	
Serial No. 09/916,527	:	Group Art Unit - 2822
Filed: July 27, 2001	:	Examiner - Kiesha L. Rose
For: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING SAME	:	Docket No. S004-4335

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BRIEF ON APPEAL

S I R:

An appeal has been taken from the final rejection of claims 1-4, 10-20, 24-31 and 34-36, and appellants present herewith their brief in support of the appeal.

(1) Real Party of Interest:

The real party of interest in this appeal is Seiko Instruments Inc.

(2) Related Appeals and Interferences:

Appellants and appellants' counsel are aware of no other appeals or interferences which will directly affect or

be directly affected by or have a direct bearing upon the Board's decision in the present appeal.

(3) Status of Claims:

The present application was filed with claims 1-33. Claims 34-36 were added by amendment and claims 5-9, 21-23, and 32-33 were canceled. Claims 1-4, 10-15, 17-20, 24-31 and 34-36 stand finally rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,296,726 to MacElwee in view of U.S. Patent No. 6,372,585 to Yu[1]. Claim 16 stands finally rejected under 35 U.S.C. §103(a) as being unpatentable over MacElwee in view of Yu[2] and further in view of U.S. Patent No. 5,708,284 to Onishi. Claim 1 also stands finally

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[1] While not indicated by the Examiner in the heading (pg. 3) of this rejection in the final Office Action, the body (pgs. 4-5) of this rejection in the final Office Action refers to U.S. Patent No. 6,372,585 to Yu which is relied upon by the Examiner for its disclosure of a polysilicon layer implanted with boron or BF_2. For the purpose of this appeal, appellants presume that the Examiner intended to reject claims 1-4, 10-15, 17-20, 24-31 and 34-36 under 35 U.S.C. §103(a) as being unpatentable over MacElwee in view of Yu.

[2] See footnote 1. This rejection also presumably relies upon Yu for its disclosure of a polysilicon layer implanted with boron or BF_2 which, as acknowledged by the Examiner on page 4 of the final Office Action, is not disclosed or suggested by MacElwee. Thus, for the purpose of this appeal, appellants presume that the Examiner intended to reject claim 16 under 35 U.S.C. §103(a) as being unpatentable over MacElwee in view of Yu and further in view of U.S. Patent No. 5,708,284 to Onishi.

rejected under the judicially created doctrine of double patenting over claim 1 of U.S. Patent No. 6,369,409 to Takasu et al. ("Takasu"). The present appeal is directed to the final rejection of claims 1-4, 10-20, 24-31 and 34-36. No claim stands allowed.

(4) Status of Amendments:

In response to a final Office Action dated March 25, 2003, an amendment after final was filed by certificate of mail dated June 24, 2003. In an Advisory Action dated July 29, 2003, the Examiner indicated that the amendment after final would be entered but that the final rejections would be maintained. No subsequent amendment after final was filed and no amendment stands unentered.

(5) Summary of Invention:

The present invention is directed to a semiconductor device.

In conventional bleeder resistance circuits using thin film resistors, there is a problem that a voltage division ratio frequently becomes inaccurate. Furthermore, in a conventional bleeder resistance circuit incorporating a MOS transistor in the same chip, there has been a problem that a resistance value change due to the temperature of polysilicon thin film resistors is large in a region of high sheet

resistance value, and the sheet resistance value has to be set small in order to obtain high voltage division accuracy in a wide temperature range. As a result, the area occupied by the bleeder circuit region requiring a high resistance value at one meg-ohm or higher becomes larger.

The present invention overcomes the drawbacks of the conventional art. Fig. 2 shows an embodiment of the semiconductor device according to the present invention embodied in the claims. The semiconductor device has thin film resistors 105-107 connected in series to form a bleeder resistance circuit. Each of the thin film resistors 105-107 is made of a polysilicon film doped with B or BF_2 P-type impurities and has two end portions each having a high impurity concentration region (P^+ region). A first insulating film 404 overlies the thin film resistors 105-107. First conductors 201-203 are connected to the ends of the thin film resistors 105-107 for connecting the thin film resistors in series. Each of second conductors 401-403 is connected to a respective one of the first conductors 201-203 and overlies a respective one of the thin film resistors 105-107 through the first insulating film 404.

Preferably, a second insulating film 405 overlies the thin film resistor 105-107. The first conductors 201-203 are connected to the thin film resistors 105-107 and to the second conductors 401-403 so that each of the thin film

resistors 105-107 is at the same potential as a respective one of the first conductors 201-203 and a respective one of the second conductors 401-403.

By the foregoing construction, a semiconductor device is provided which has a bleeder resistance circuit of high accuracy and having an accurate voltage division ratio and a small temperature coefficient of a resistance value.

(6) Issue:

A primary issue presented by this appeal is whether the Examiner has made out a prima facie case of obviousness of the subject matter of claims 1-4, 10-15, 17-20, 24-31 and 34-36 in view of the teachings of MacElwee in combination with those of Yu[3].

Another primary issue presented by this appeal is whether the Examiner has made out a prima facie case of obviousness of the subject matter of claim 16 in view of the teachings of MacElwee in combination with those of Yu[4] and Onishi.

Yet another primary issue presented by this appeal is whether the subject matter of claim 1 is fully disclosed in claim 1 of Takasu under the judicially created doctrine of double patenting.

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[3] See footnote 1.

[4] See footnote 2.

(7) Grouping of Claims:

In the final Office Action, claims 1-4, 10-15, 17-20, 24-31 and 34-36 were grouped together in one ground of rejection under 35 U.S.C. §103(a). Claim 16 was grouped in another ground of rejection under 35 U.S.C. §103(a). Claim 1 was also grouped under another ground of rejection based on the judicially created doctrine of double patenting.

Appellants respectfully submit that the rejected claims fall in the following groups, the claims in each group being separately patentable for the reasons given below in section (8):

(a) Independent claim 1 and dependent claims 3, 4, 10-20 and 24-31;

(b) Dependent claim 2;

(c) Independent claim 34 and dependent claim 35; and

(d) Dependent claim 36.

(8) Argument:

Claims 1-4, 10-15, 17-20, 24-31 and 34-36 stand finally rejected under 35 U.S.C. §103(a) as being unpatentable over MacElwee in view of Yu[5]. Appellants respectfully traverse this rejection and submit that the combined teachings

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[5] See footnote 1.

of MacElwee and Yu do not disclose or suggest the subject matter recited in independent claims 1, 34 and dependent claims 2-4, 10-15, 17-20, 24-31 and 35-36.

Independent claim 1 is directed to a semiconductor device and requires a plurality of thin film resistors connected in series to form a bleeder resistance circuit, each of the thin film resistors being made of a polysilicon film doped with B or BF_2 P-type impurities and having two end portions each having a high impurity concentration region. Independent claim 1 further requires a first insulating film overlying the thin film resistors, a plurality of first conductors connected to the ends of the thin film resistors for connecting the thin film resistors in series, and a plurality of second conductors each connected to a respective one of the first conductors and overlying a respective one of the thin film resistors through the first insulating film. No corresponding combination is disclosed or suggested by the combined teachings of MacElwee and Yu.

Independent claim 34 is also directed to a semiconductor device and requires a plurality of thin film resistors overlying the first insulating film and electrically connected in series by the first conductors, each of the thin film resistors being made of a polysilicon film doped with B or BF_2 P-type impurities and overlying a respective one of the first conductors. Again, no corresponding combination is

disclosed or suggested by combined teachings of MacElwee and Yu.

The primary reference to MacElwee discloses a resistive load structure having two thin film accumulation mode field effect transistors connected in series with a common node and separate gate electrodes. Contrary to the Examiner's contention in the final Office Action and in the Advisory Action, MacElwee does not disclose or suggest a plurality of thin film resistors electrically connected in series, as required by independent claim 1 and 34. Likewise, as recognized by the Examiner on page 4 of the final Office Action, MacElwee does not disclose or suggest that each of the thin film resistors is made of a polysilicon film doped with B or BF_2 P-type impurities, as required by independent claims 1 and 34. For example, as shown in Fig. 2 of MacElwee, a polysilicon layer 50 is selectively doped by ion implantation to form heavily doped N+ regions 54 and heavily doped N+ region 56, leaving relatively lightly doped resistive regions 58 (col. 5, lines 9-16). Thus MacElwee clearly does not disclose or suggest a plurality of P-type polysilicon thin film resistors connected in series, as required by independent claims 1 and 34.

Moreover, independent claim 1 requires that the P-type polysilicon thin film resistors are connected in series to form a bleeder resistance circuit. No corresponding

electrical structure is disclosed or suggested by MacElwee. For example, in Fig. 1 of MacElwee a resistor 10 comprises a body formed from a resistive conductive layer of polysilicon which is lightly p- or n-doped to provide a resistive region 12 having a desired resistivity range (col. 4, lines 42-45). The resistor 10 in MacElwee clearly does not constitute a bleeder resistance circuit, as required by independent claim 1.

The Examiner cited the secondary reference to Yu for its disclosure of a semiconductor device containing a polysilicon layer implanted with boron or BF_2. However, as recognized by the Examiner, Yu does not disclose or suggest a plurality of P-type polysilicon thin film resistors connected in series, as required by independent claims 1 and 34. Likewise, Yu does not disclose or suggest P-type polysilicon thin film resistors are connected in series to form a bleeder resistance circuit, as required by independent claim 1. Since Yu does not disclose or suggest these structural features, it does not cure the deficiencies of MacElwee.

It is well established that in assessing patentability of a claimed invention, all claim limitations must be suggested or taught by the prior art. In re Royka, 180 USPQ 580 (CCPA 1974). In this case, MacElwee and Yu, either alone or in combination, do not disclose or suggest all of the limitations recited in independent claims 1 and 34 as set forth above.

Claims 2-4, 10-15, 17-20, 24-31 and 35-36 depend on and contain all of the limitations of independent claims 1 and 34, respectively, and, therefore, distinguish from the references at least in the same manner as claims 1 and 34.

Moreover, there are separate grounds for patentability of dependent claims 2 and 36.

With reference to the embodiment of the present invention shown in Fig. 2, amended claim 2 includes the additional limitation that a second insulating film 405 overlies the thin film resistors 105-107, and that the first conductors 201-203 are connected to the thin film resistors 105-107 and to the second conductors 401-403 so that each of the thin film resistors 105-107 is at the same potential as a respective one of the first conductors 201-203 and a respective one of the second conductors 401-403. Claim 36 requires a second insulating film overlying the plurality of thin film resistors, a plurality of second conductors formed on the second insulating film and each overlying a respective one of the thin film resistors, and second connecting means conductively connecting one end of each the thin film resistors to a respective one of the second conductors so that each of the thin film resistors is at the same potential as the respective one of the second conductors.

The prior art of record does not disclose or suggest the subject matter recited in independent claims 2 and 36. For example, MacElwee discloses an insulating film (i.e., a

dielectric layer) 60 overlying a resistor 50 (Fig. 1). However, MacElwee does not disclose or suggest a second insulating film overlying the resistor 50.

Moreover, while acknowledging that MacElwee does not disclose or suggest first conductors connected to thin film resistors and to second conductors so that each of the thin film resistors is at the same potential as a respective one of the first conductors and a respective one of the second conductors, the Examiner has taken official notice that application of "the same voltage to the conductors and the thin film resistors will make them have the same potential" to support its conclusion of obviousness. Appellants respectfully disagree with the Examiner's reliance on only officially noticed facts to support the conclusion that it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a semiconductor device having first conductors connected to thin film resistors and to second conductors so that each of the thin film resistors is at the same potential as a respective one of the first conductors and a respective one of the second conductors, as required by appealed claims 2 and 36.

Appellants respectfully submit that officially noticed facts may only play a minor role in filling evidentiary gaps to support a conclusion of obviousness and cannot provide the totality of evidence to support an

obviousness rejection. In re Ahlert, 165 USPQ 418, 421 (CCPA 1970). See, also, In re Kaplan, 229 USPQ 678, 683 (Fed. Cir. 1986) ("Even if obviousness of the variation is predicated on the level of skill in the art, prior art evidence is needed to show what that level of skill was.").

In this case, the Examiner has failed to establish a recognition in the prior art, and thus knowledge thereof, of providing a semiconductor device having first conductors connected to thin film resistors and to second conductors so that each of the thin film resistors is at the same potential as a respective one of the first conductors and a respective one of the second conductors, as recited in claims 2 and 36. Thus the Examiner cannot properly rely on a conclusion of obviousness solely on official notice to arrive at the invention recited in claims 2 and 36.

Accordingly, appellants respectfully submit that claims 1-4, 10-15, 17-20, 24-31 and 34-36 patentably distinguish over the prior art of record and that the rejection of the claims under 35 U.S.C. §103(a) should be reversed.

Claim 16 was rejected under 35 U.S.C. §103(a) as being unpatentable over MacElwee in view of Yu[6] and further in view of Onishi. Appellants respectfully traverse this

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[6] See footnote 2.

rejection and submit that the combined teachings of MacElwee, Yu and Onishi do not disclose or suggest the subject matter recited in claim 16.

MacElwee in view of Yu does not disclose or suggest the subject matter recited in amended independent claim 1 as set forth above for the rejection of claims 1-4, 10-15, 17-20, 24-31 and 34-36 under 35 U.S.C. §103(a). Claim 16 depends on and contains all of the limitations of amended independent claim 1 and, therefore, distinguishes from the reference at least in the same manner as claim 1.

The secondary reference to Onishi was cited by the Examiner for its disclosure of a memory device containing a conductor layer formed of a lamination layer containing a barrier metal and a silicide layer. However, Onishi clearly does not disclose or suggest the structure of the semiconductor device recited in amended independent claim 1, including the recited structure of the thin film resistors and the recited structural relationship among the thin film resistors, first insulating film and first and second conductors. Since Onishi does not disclose or suggest these features, it does not cure the deficiencies of MacElwee in view of Yu.

Accordingly, appellants respectfully submit that claim 16 patentably distinguishes over the prior art of record and that the rejection of this claim under 35 U.S.C. §103(a) should be reversed.

Independent claim 1 was further rejected under the judicially created doctrine of double patenting over claim 1 of Takasu. Appellants respectfully submit that independent claim 1 is patentably distinct from claim 1 of Takasu.

Independent claim 1 requires a plurality of thin film resistors connected in series to form a bleeder resistance circuit, each of the thin film resistors being made of a polysilicon film doped with B or BF_2 P-type impurities. While reciting a plurality of polysilicon thin film resistors, claim 1 of Takasu does not recite that <u>each of the thin film resistors is made of a polysilicon film doped with B or BF_2 P-type impurities</u>, as required by independent claim 1. Accordingly, independent claim 1 patentably distinguishes from claim 1 of Takasu.

In view of the foregoing, appellants respectfully request that the rejection of claim 1 under the judicially created doctrine of double patenting over claim 1 of Takasu be reversed.

In view of the foregoing, appellants respectfully submit that claims 1-4, 10-20, 24-31 and 34-36 patentably distinguish over the prior art record and, therefore, the prior art rejections of these claims should not be sustained.

Respectfully submitted,

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(9) **Appendix**

Appealed claims 1-4, 10-20, 24-31 and 34-36 are reproduced below in smooth form:

1. A semiconductor device comprising: a plurality of thin film resistors connected in series to form a bleeder resistance circuit, each of the thin film resistors being made of a polysilicon film doped with B or BF_2 P-type impurities and having two end portions each having a high impurity concentration region; a first insulating film overlying the thin film resistors; a plurality of first conductors connected to the ends of the thin film resistors for connecting the thin film resistors in series; and a plurality of second conductors each connected to a respective one of the first conductors and overlying a respective one of the thin film resistors through the first insulating film.

2. A semiconductor device according to claim 1; further comprising a second insulating film overlying the thin film resistors; wherein the first conductors are connected to the thin film resistors and to the second conductors so that each of the thin film resistors is at the same potential as a respective one of the first conductors and a respective one of the second conductors.

3. A semiconductor device according to claim 1; wherein each of the first conductors is at the same potential as a respective one of the thin film resistors.

4. A semiconductor device according to claim 2; wherein each of the second conductors is at the same potential as a respective one of the thin film resistors.

10. A semiconductor device according to claim 1; wherein the film thickness of each of the thin film resistors is several tens to 2000 angstroms.

11. A semiconductor device according to claim 1; wherein the film thickness of each of the thin film resistors is several tens to 1000 angstroms.

12. A semiconductor device according to claim 1; wherein the first conductors are composed of well regions formed in a silicon substrate.

13. A semiconductor device to claim 1; wherein the first conductors are made of polysilicon.

14. A semiconductor device according to claim 1; wherein the second conductors are made of polysilicon.

15. A semiconductor device according to claim 1; wherein the second conductors are made of aluminum.

16. A semiconductor device according to claim 1; wherein the second conductors are made from a lamination film of a barrier metal and a silicide film.

17. A semiconductor device according to claim 1; wherein the first conductors are made of a material forming a gate electrode of a MOS transistor formed on the same chip as the thin film transistors.

18. A semiconductor device according to claim 1; wherein potentials of each of the plurality of thin film resistors and the first conductors connected to them are fixed by a metal wiring material through a common contact hole.

19. A semiconductor device according to claim 1; further comprising a MOS transistor having a gate electrode; and wherein a film thickness of each of the thin film resistors is formed thinner than a film thickness of the gate electrode of the MOS transistor.

20. A semiconductor device according to claim 19; wherein the film thickness of the thin film resistors is several tens to 1000 angstroms.

24. A semiconductor device according to claim 19; wherein a temperature dependency of the resistance value of the thin film resistors is -4000 ppm/°C or lower.

25. A semiconductor device according to claim 1; wherein each of the thin film resistors has a low resistance region having the high impurity concentration for connecting with metal wiring, and a high resistance region; and wherein a film thickness of the high resistance region is smaller than that of the low resistance region.

26. A semiconductor device according to claim 25; wherein the film thickness of the high resistance region is several tens to 1000 angstroms and the film thickness of the low resistance region is 2000 to 10000 angstroms.

27. A semiconductor device according to claim 25; wherein the low resistance region and the high resistance region of the thin film resistors are formed on a common flat surface.

28. A semiconductor device according to claim 25; wherein upper surfaces of the low resistance region and the high resistance region of the thin film resistors form the same flat surface.

29. A semiconductor device according to claim 2; wherein the first insulating film and the second insulating film are made of a silicon oxide films.

30. A semiconductor device according to claim 2; wherein one or both of the first insulating film and the second insulating film are made of a multilayer film containing a silicon nitride film.

31. A semiconductor device according to claim 1; wherein a resistance value of the entire bleeder resistance circuit using the plurality of thin film resistors is 1 mega-ohm to 100 mega-ohms.

34. A semiconductor device comprising:

a plurality of first conductors;

a first insulating film overlying the first conductors;

a plurality of thin film resistors overlying the first insulating film and electrically connected in series by the first conductors, each of the thin film resistors being made of a polysilicon film doped with B or BF_2 P-type impurities and overlying a respective one of the first conductors; and

first connecting means for electrically connecting each of the first conductors to an end of a respective one of the thin film resistors so that each of the first conductors is at the same potential as the respective one of the thin film resistors.

35. A semiconductor device according to claim 34; wherein each of the thin film resistors has two ends, the thin film resistors being spaced from one another along a line and the two ends of each of the resistors being spaced apart along the line.

36. A semiconductor device according to claim 35; further comprising a second insulating film overlying the plurality of thin film resistors; a plurality of second conductors formed on the second insulating film and each overlying a respective one of the thin film resistors; and second connecting means conductively connecting one end of each the thin film resistors to a respective one of the second conductors so that each of the thin film resistors is at the same potential as the respective one of the second conductors.